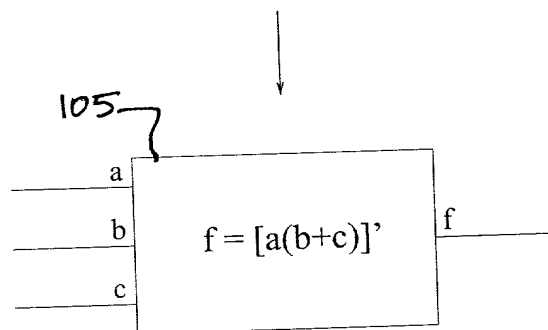


AVAILABLE CELL



TARGET FUNCTION

$$f = [xy + zy]'$$

FIG. 1

FUNCTIONAL MATCHES

MATCH_1		MATCH_2	
a	y	a	y
b	x	b	z
c	z	c	x

FIG. 1a

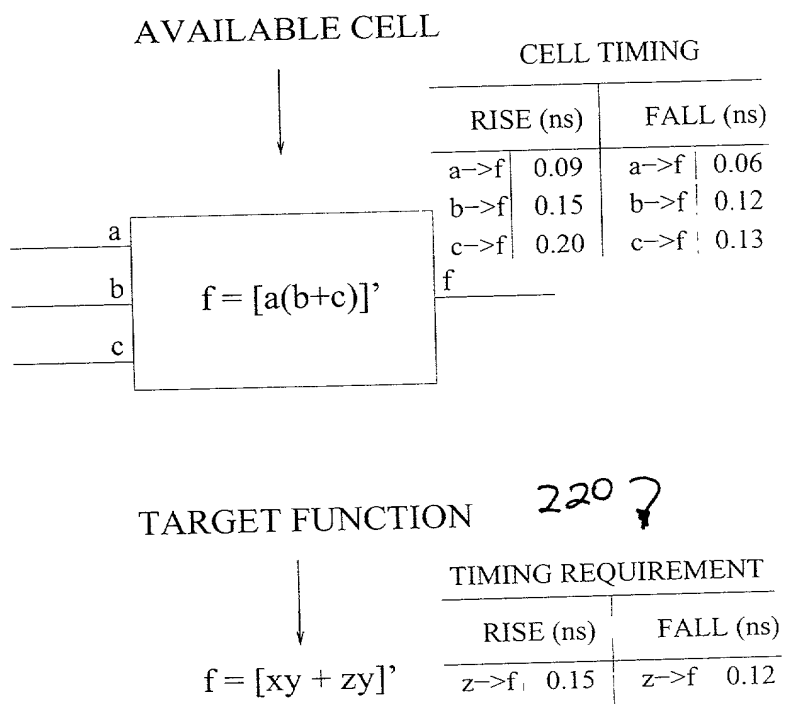


FIG. 2

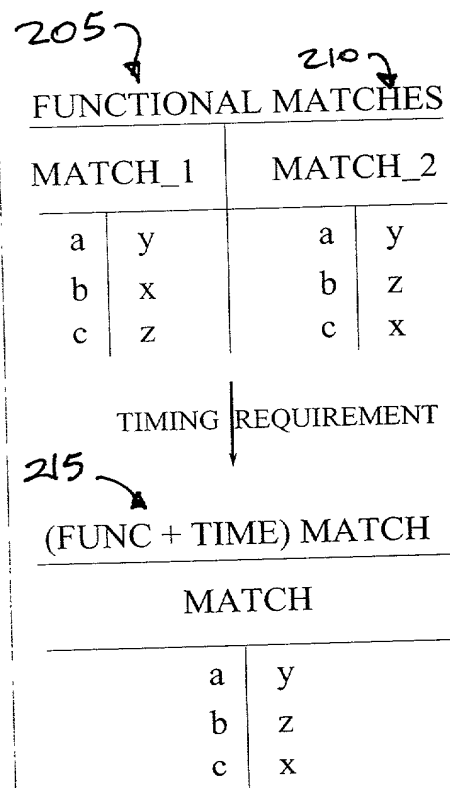


FIG. 2a

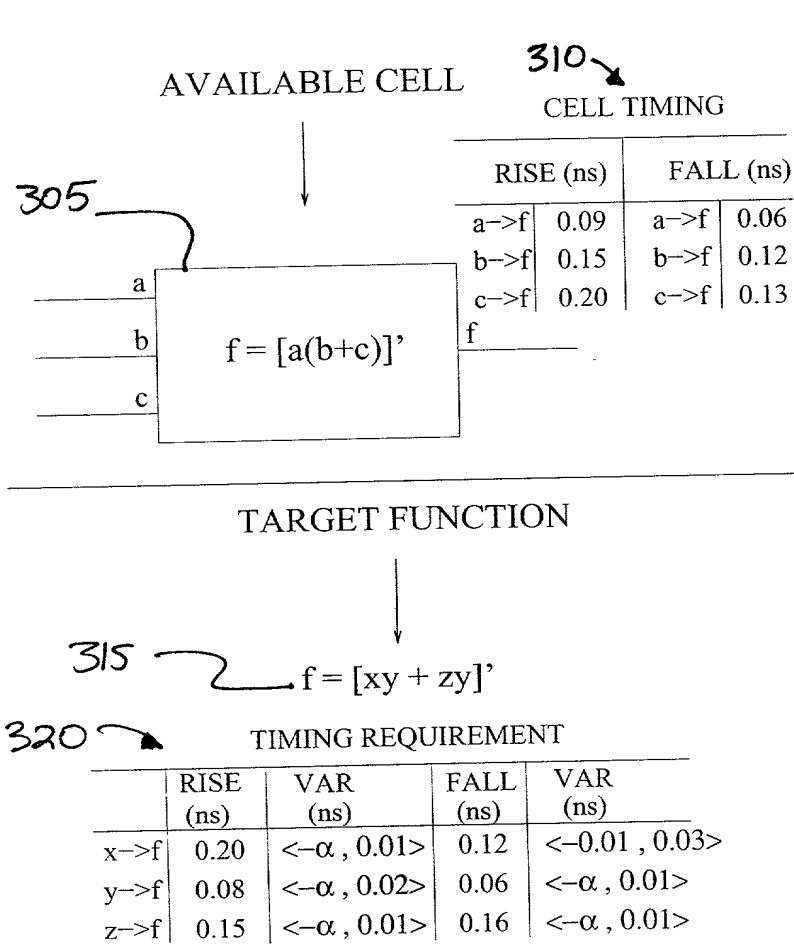


FIG. 3

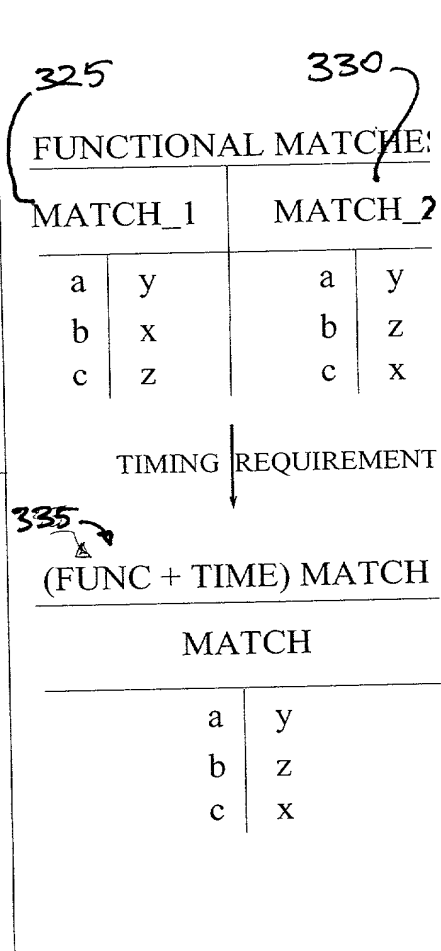


FIG. 3a

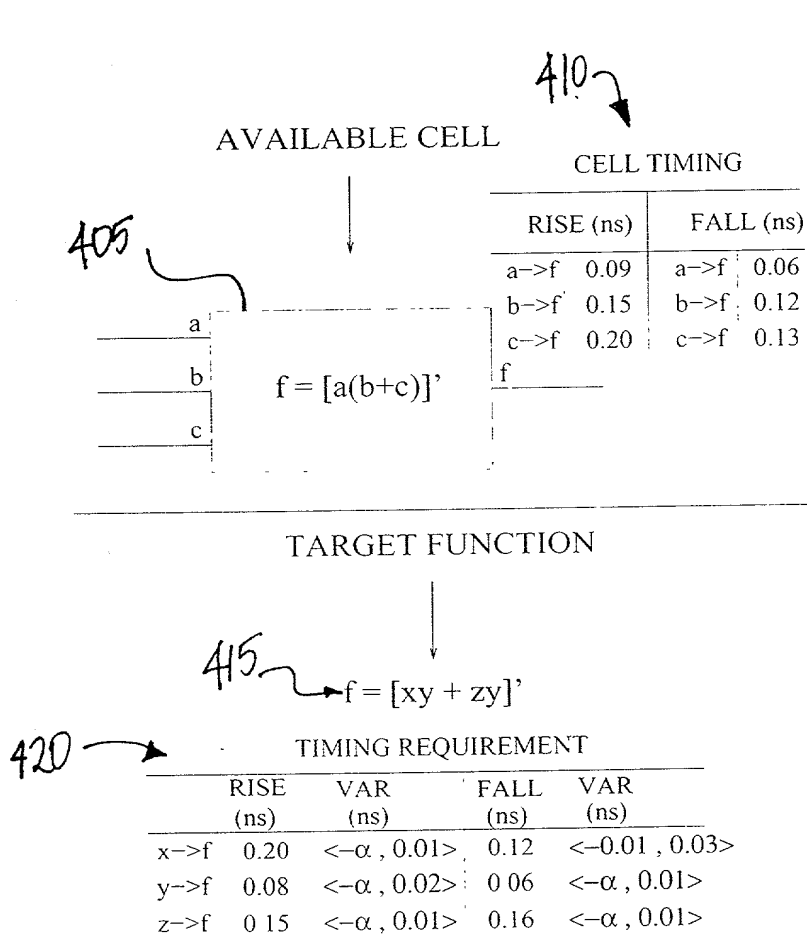


FIG. 4

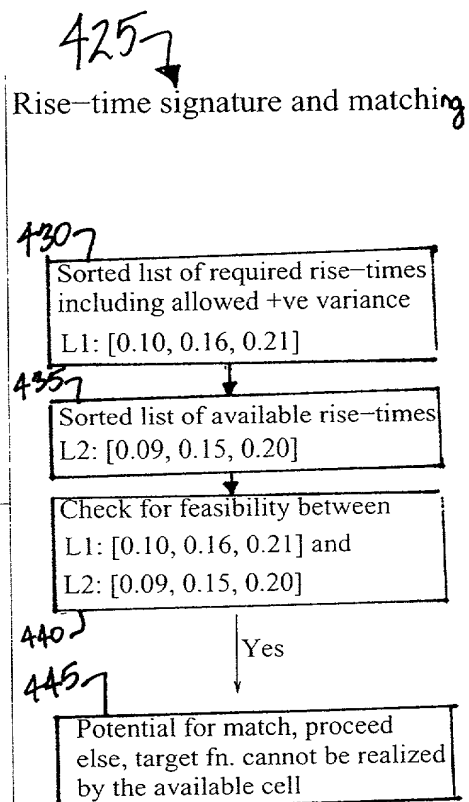


FIG. 4a

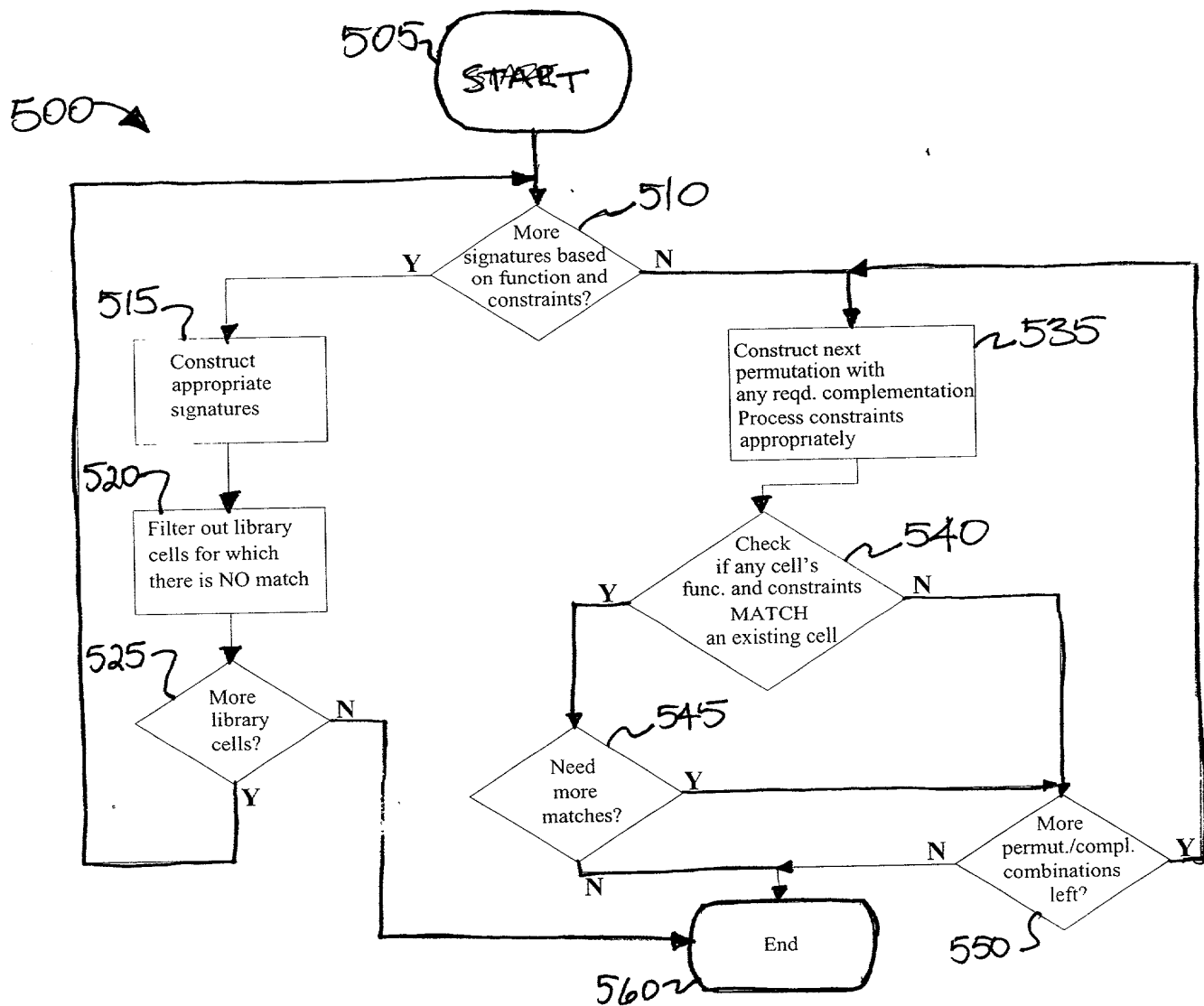
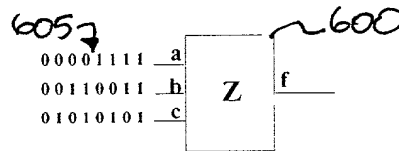


FIG. 5

If context is NOT known,  
ALL input values need to be considered



If context is known,  
ONLY SOME input values need to be considered

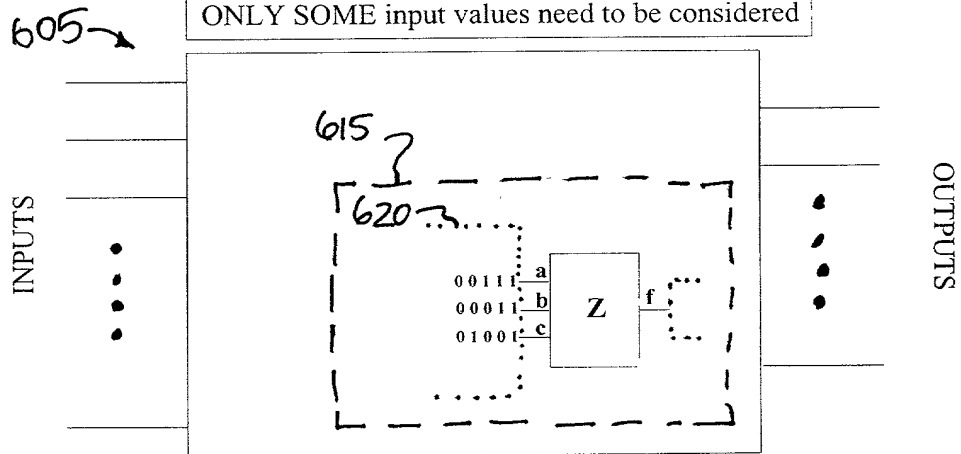
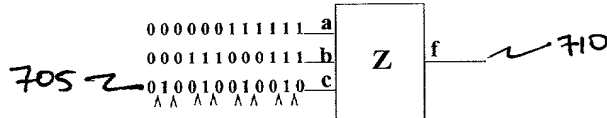


FIG. 6

If context is NOT known,  
To characterize timing on c→f  
ALL possible 0→1 and 1→0 transitions  
on C need to be considered



If context is known,  
To characterize timing on c→f  
ONLY SOME 0→1 and 1→0 transitions  
on C need to be considered  
(Context eliminates other transitions)

- Characterization is MORE accurate
- Characterization needs LESSER resources

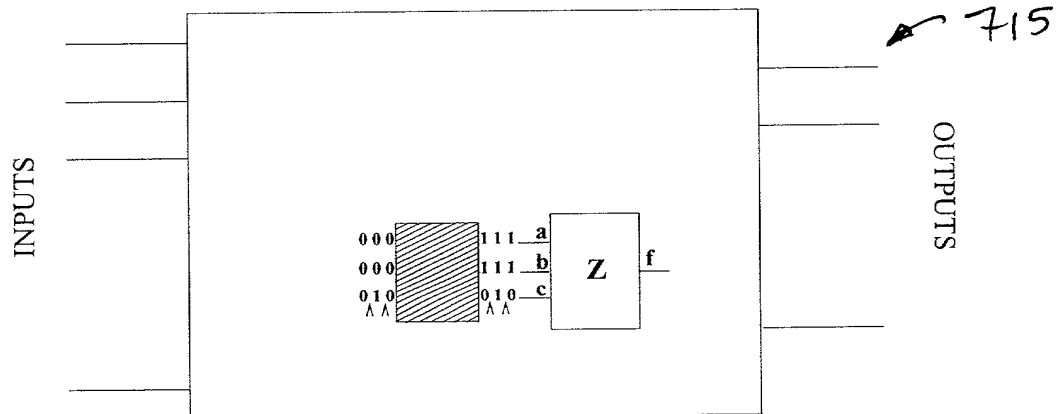
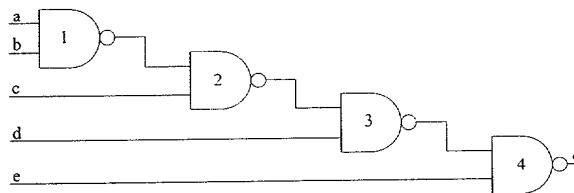


FIG. 7

800 →



805 →

Worst propagation delay through the design

Drive strengths					Gate-level	Transistor-level
at stage					timing (STA)	timing (SPICE)
1	2	3	4		(ns)	(ns)
0	0	0	0		0.40	0.186
1	1	1	1		0.22	0.166
2	2	2	2		0.15	0.157
4	4	4	4		0.61	0.581
0	1	2	4		0.41	0.332

Figure 8: Example to illustrate that characterization at the transistor-level is more accurate than that done by gate-level static timing analysis

FIG. 8



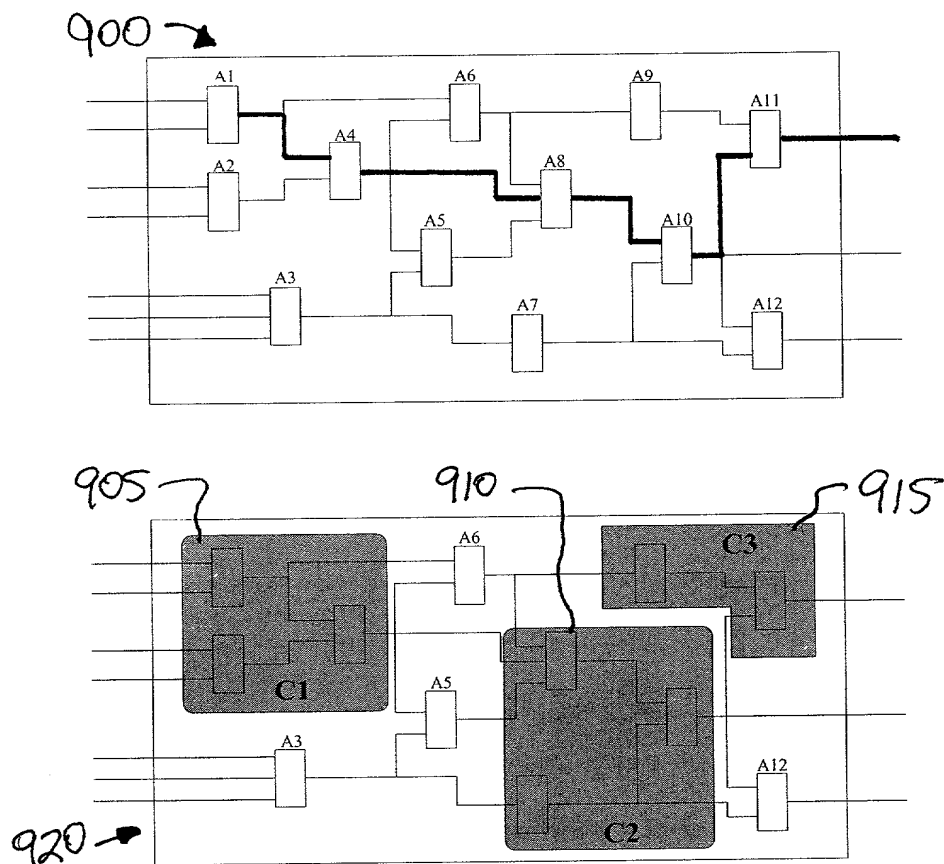


FIG. 9